CLAIMS

[0060] What is claimed as new and desired to be protected by Letters Patent of the United States is:

1. A circuit for coordinating refresh and parity-scan operations in a memory device, said circuit comprising:

a plurality of register fields, said register fields containing at least configuration information regarding the memory device; and

control logic coupled to the register fields, said control logic using the information in the register fields to determine whether parity-scan operations can be substituted for refresh operations and scheduling the parity-scan operations when it is determined that the parity-scan operations can be substituted for refresh operations.

2. The circuit of claim 1, wherein said control logic schedules refresh operations if it is determined that parity-scan operations cannot be substituted for refresh operations.

3. The circuit of claim 1, wherein said plurality of register fields comprise configuration register fields containing configuration information.

4. The circuit of claim 3, wherein said plurality of register fields further comprise command register fields containing command information.

5. The circuit of claim 4, wherein said plurality of register fields further comprise status register fields containing status information.

6. The circuit of claim 1, wherein said plurality of register fields comprise:

configuration register fields containing configuration information;

command register fields containing command information; and

status register fields containing status information.

7. The circuit of claim 1, wherein said control logic comprises:

a comparator coupled to said registers, said comparator comparing a maximum refresh interval with a maximum parity-scan interval, said comparator outputting a smallest value of said intervals;

counting logic that tracks a next row to be refreshed or parity scanned based at least on the smallest value and a total number of rows to be scanned;

self-refresh logic coupled to the counting logic and being enabled or disable by information within said registers;

parity-scan logic coupled to the counting logic and being enabled or disable by information within said registers; and

coordinating logic for using the information within the registers to control the self-refresh and parity-scan logic.

8. The circuit of claim 7, wherein said coordinating logic checks a command stream for idle cycles to insert parity-scan or refresh commands into.

9. The circuit of claim 7 further comprising a multiplexer for selecting an output from said self-refresh logic and said parity-scan logic based on a signal from said coordinating logic.

10. The circuit of claim 7 further comprising:

a first status register field for storing row address information; and

a second status register field for indicating that all rows have been scanned before the end of a scan period.

11. A memory device comprising:

a plurality of memory cells organized as an array of rows and columns;

a plurality of register fields, said register fields containing information regarding the memory device; and

control logic coupled to the register fields for coordinating refresh and parity-scan operations on the memory cells, said control logic using the information in the register fields to schedule parity-scan operations as a substitute for refresh operations when it is determined that the parity-scan operations can be substituted for refresh operations.

12. The memory device of claim 11, wherein said control logic schedules refresh operations if it is determined that parity-scan operations cannot be substituted for refresh operations.

13. The memory device of claim 11, wherein said plurality of register fields comprise configuration register fields containing configuration information.

14. The memory device of claim 11, wherein said plurality of register fields comprise command register fields containing command information.

15. The memory device of claim 11, wherein said plurality of register fields comprise status register fields containing status information.

16. The memory device of claim 11, wherein said plurality of register fields comprise:

configuration register fields containing configuration information;

command register fields containing command information; and

status register fields containing status information.

17. The memory device of claim 11, wherein said control logic comprises:

a comparator coupled to said registers, said comparator comparing a maximum refresh interval with a maximum parity-scan interval, said comparator outputting a smallest value of said intervals;

counting logic that tracks a next row to be refreshed or parity scanned based at least on the smallest value and a total number of rows to be scanned;

self-refresh logic coupled to the counting logic and being enabled or disable by information within said registers;

parity-scan logic coupled to the counting logic and being enabled or disable by information within said registers; and

coordinating logic for using the information within the registers to control the self-refresh and parity-scan logic.

18. The memory device of claim 17, wherein said coordinating logic checks a command stream for idle cycles to insert parity-scan or refresh commands into.

19. The memory device of claim 17 further comprising a multiplexer for selecting an output from said self-refresh logic and said parity-scan logic based on a signal from said coordinating logic.

20. The memory device of claim 11 further comprising:

a first status register field for storing row address information; and

a second status register field for indicating that all rows have been scanned before the end of a scan period.

21. The memory device of claim 11, wherein said memory cells are dynamic random access memory cells.

22. The memory device of claim 11, wherein said memory cells are content addressable memory cells comprised of dynamic random access memory.

23. A memory device comprising:

a plurality of register fields, said register fields containing information regarding the memory device; and

means for substituting parity-scan operations on memory cells of the memory device for refresh operations.

24. The memory device of claim 23 further comprising an array of dynamic random access memory cells.

25. The memory device of claim 23 further comprising an array of content addressable memory cells comprised of dynamic random access memory.

26. A processor system comprising:

a processor; and

a memory device coupled to said processor, said memory device comprising a circuit for coordinating refresh and parity-scan operations in said memory device, said circuit comprising:

a plurality of register fields, said register fields containing at least configuration information regarding the memory device; and

control logic coupled to the register fields, said control logic using the information in the register fields to determine whether parity-scan operations can be substituted for refresh operations and scheduling the parity-scan operations when it is determined that the parity-scan operations can be substituted for refresh operations.

27. The system of claim 26, wherein said control logic schedules refresh operations if it is determined that parity-scan operations cannot be substituted for refresh operations.

28. The system of claim 26, wherein said plurality of register fields comprise configuration register fields containing configuration information.

29. The system of claim 26, wherein said plurality of register fields further comprise command register fields containing command information.

30. The system of claim 26, wherein said plurality of register fields further comprise status register fields containing status information.

31. The system of claim 26, wherein said plurality of register fields comprise:

configuration register fields containing configuration information;

command register fields containing command information; and

status register fields containing status information.

32. The system of claim 26, wherein said control logic comprises:

a comparator coupled to said registers, said comparator comparing a maximum refresh interval with a maximum parity-scan interval, said comparator outputting a smallest value of said intervals;

counting logic that tracks a next row to be refreshed or parity scanned based at least on the smallest value and a total number of rows to be scanned;

self-refresh logic coupled to the counting logic and being enabled or disable by information within said registers;

parity-scan logic coupled to the counting logic and being enabled or disable by information within said registers; and coordinating logic for using the information within the registers to control the self-refresh and parity-scan logic.

33. The system of claim 32, wherein said coordinating logic checks a command stream for idle cycles to insert parity-scan or refresh commands into.

34. The system of claim 32 further comprising a multiplexer for selecting an output from said self-refresh logic and said parity-scan logic based on a signal from said coordinating logic.

35. The system of claim 32 further comprising:

a first status register field for storing row address information; and

a second status register field for indicating that all rows have been scanned before the end of a scan period.

36. A processor system comprising:

a processor; and

a memory device connected to the processor, said memory device comprising:

a plurality of memory cells organized as an array of rows and columns;

a plurality of register fields, said register fields containing information regarding the memory device; and

control logic coupled to the register fields for coordinating refresh and parity-scan operations on the memory cells, said control logic using the information in the register fields to schedule parity-scan operations as a substitute for refresh operations when it is determined that the parity-scan operations can be substituted for refresh operations.

37. The system of claim 36, wherein said control logic schedules refresh operations if it is determined that parity-scan operations cannot be substituted for refresh operations.

38. The system of claim 36, wherein said plurality of register fields comprise configuration register fields containing configuration information.

39. The system of claim 36, wherein said plurality of register fields comprise command register fields containing command information.

40. The system of claim 36, wherein said plurality of register fields comprise status register fields containing status information.

41. The system of claim 36, wherein said plurality of register fields comprise:

configuration register fields containing configuration information;

command register fields containing command information; and

status register fields containing status information.

42. The system of claim 36, wherein said control logic comprises:

a comparator coupled to said registers, said comparator comparing a maximum refresh interval with a maximum parity-scan interval, said comparator outputting a smallest value of said intervals;

counting logic that tracks a next row to be refreshed or parity scanned based at least on the smallest value and a total number of rows to be scanned;

self-refresh logic coupled to the counting logic and being enabled or disable by information within said registers;

parity-scan logic coupled to the counting logic and being enabled or disable by information within said registers; and coordinating logic for using the information within the registers to control the self-refresh and parity-scan logic.

43. The system of claim 42, wherein said coordinating logic checks a command stream for idle cycles to insert parity-scan or refresh commands into.

44. The system of claim 42, further comprising a multiplexer for selecting an output from said self-refresh logic and said parity-scan logic based on a signal from said coordinating logic.

45. The system of claim 42, further comprising:

a first status register field for storing row address information; and

a second status register field for indicating that all rows have been scanned before the end of a scan period.

46. The system of claim 36, wherein said memory cells are dynamic random access memory cells.

47. The system of claim 36, wherein said memory cells are content addressable memory cells comprised of dynamic random access memory.

48. A processor system comprising:

a processor; and

a memory device connected to the processor, said memory device comprising:

a plurality of register fields, said register fields containing information regarding the memory device; and

means for substituting parity-scan operations on memory cells of the memory device for refresh operations.

49. A router comprising:

a plurality of register fields, said register fields containing information regarding the memory device; and

means for substituting parity-scan operations on memory cells of the memory device for refresh operations.

50. A method of coordinating refresh and parity-scanning in a memory array, comprising:

determining whether parity-scan operations can be substituted for refresh operations; and

scheduling the parity-scan operations when it is determined that the parity-scan operations can be substituted for refresh operations.

51. The method of claim 50 further comprising the step of scheduling the refresh operations when it is determined that the parity-scan operations cannot be substituted for refresh operations.

52. The method of claim 50 further comprising the step of checking parities returned from the memory array to ensure data integrity.

53. The method of claim 50, wherein the determining step comprises:

selecting a smallest parameter of a maximum refresh interval and a maximum parity-scan interval;

dividing the selected parameter by the number of rows per bank to generate a wrap-around limit;

sending an increment signal to a counter when said wrap-around limit is met;

tracking a next row to be refreshed or parity-scanned with said counter;

generating command, enable and address values;

selecting a value indicative of the operation to be performed; and

checking the command stream for idle cycles to insert parity-scan or refresh.